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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,566	MADRID ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/05/2002;7/19/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 26 are presented for examination.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 7 and 8 are objected to because of the following informalities:

4. In the claim 7, replace "said registers" with ---said shift registers----

5. In the claim 8, replace "said registers" with ---said shift registers----.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 1, is rejected under 35 U.S.C. 102(e) as being anticipated by Ilan et al. [hereinafter as Ilan], US 6,629,256 B1.

7. As to claim 1, Ilan discloses a method comprising:

a. generating a first clock signal [f_{avail} by a clock source number 2] with a first frequency [available clock source frequency]; and

b. utilizing said first clock signal [f_{avail}] to generate a second clock signal [f_{stdby}] with a second frequency [standby frequency clock];

wherein said second clock frequency [f_{stdby}] is generated by dropping [swallowing] selected pulses [predetermined number of cycles] of said first clock signal [f_{avail}][col. 2, lines 12 – 23, col. 3, lines 1 – 30, fig. 2].

8. Claims 1 – 2, 4 – 6, 9 – 10, 12 – 14, 17 – 19, 21 – 22, and 25 - 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Svensson et al. [hereinafter as Svensson], US 6,711,694 B1.

9. As to claim 1, Svensson discloses a method comprising:

a. generating a first clock signal [master clock] with a first frequency [master clock frequency]; and

b. utilizing said first clock signal [master clock] to generate a second clock signal [dithered clock] with a second frequency [dithered clock frequency];

wherein said second clock frequency [dithered clock frequency] is generated by dropping [omitting] selected pulses [selected clock pulses] of said first clock signal [master clock][col. 2, lines 18 – 26, col. 5, lines 38 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 36, fig. 6, 7].

10. As to claim 9, Svensson discloses a clock circuit comprising:

a. a first circuit [605] configured to generate a first clock signal [master clock]; and

b. circuitry [510] configured to utilize said first clock signal [masterclock] to generate a second clock signal [dithered clock] with a second frequency [dithered clock

frequency], wherein said second clock frequency [dithered clock frequency] is generated by dropping [omitting] selected pulses [selected clock pulses] of said first clock signal [master clock] [col. 2, lines 18 – 26, col. 5, lines 38 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 36, fig. 6, 7].

11. As to claim 18, Svensson discloses a system comprising:

a. a reference clock generator [605, clock generator] configured to generate a reference clock signal [master clock]; and

b. a processor [520, digital circuitry of wireless mobile terminal is inherently having a processor] comprising a clock circuit [510, fig. 5] configured to:

(i) receive said reference clock signal [from a clock source oscillator which is inherent to mobile terminal];

(ii) generate [clock generator generates] a first clock signal [master clock] from said reference clock signal [source clock]; and

(iii) utilize said first clock signal [master clock] to generate a second clock signal [dithered clock] with a second frequency [dithered frequency], wherein said second clock frequency [dithered frequency] is generated by dropping [omitting] [selected clock pulses] of said first clock signal [master clock] [col. 2, lines 18 – 26, col. 5, lines 38 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 36, fig. 5 – 7].

12. As to claims 2, 10, and 19, Svensson discloses a counter [625] utilizing a first clock signal [master clock] and a sequence of values from a storage element [col. 5, lines 45 – 67, col. 6, lines 4 – 27, lines 40 – 59, fig. 6 – 7].

13. As to claims 3, 11, and 20, Svensson discloses a shift register [using multiple flip-flops 727] [col. 6, lines 45 – 47] and selection of sequence of values [col. 6, lines 15 – 27].

14. As to claims 4, 12, and 21, Svensson discloses a counter [625] for counting sequences of pulses of the first clock [master clock] signal; and detecting said selected pulses of first clock [master clock] signal by comparing with constant values [col. 5, lines 45 – 60].

15. As to claims 5, 13, and 22, Svensson discloses sequences including a fixed number of pulses and wherein selected pulses correspond to particular counts of said pulses within fixed number of pulses [col. 6, lines 14 – 27, col. 7, lines 7 - 35].

16. As to claims 6, 14, and 23, Svensson discloses a shift register [col. 6, lines 45 – 47] therefore he teaches loading of shift registers with predetermined values too.

17. As to claim 17, Svensson discloses a wireless mobile terminal with digital circuitry [520], which inherently comprises a processor, which includes modulator [510][fig. 5].

18. As to claim 25, Svensson discloses a wireless mobile terminal with digital circuitry [520], which inherently teaches a system controller coupled to receive a reference clock [fig. 5].

19. As to claim 26, Svensson discloses a wireless mobile terminal with digital circuitry [520], which inherently teaches a system controller and coupled to a main memory, graphic adapter, and peripheral bus controller too [fig. 5].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 3, 7 – 8, 11, 15 – 16, 20, and 23 – 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Svensson et al. [hereinafter as Svensson], US 6,711,694 B1 as applied to claims 1, 10, and 18 above, and further in view of Dellow, US Patent 6, 630, 849 B2.

21. As to claims 3, 11, and 20, Svensson discloses an apparatus and method comprising: generating a first clock signal [master clock] with a first frequency [master clock frequency]; and utilizing said first clock signal [master clock] to generate a second clock signal [dithered clock] with a second frequency [dithered clock frequency]; wherein said second clock frequency [dithered clock frequency] is generated by dropping [omitting] selected pulses [selected clock pulses] of said first clock signal [master clock][col. 2, lines 18 – 26, col. 5, lines 38 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 36, fig. 6, 7].

Svensson discloses a shift register but does not teach the use of first and second [two] shift registers to store values and configured to select the sequence values from registers in an alternating manner.

Dellow discloses a two shift registers frequency divider [clock generator] with a digital clock signal [reference clock] with multiplexer arrangement to select values from shift registers in alternating manner to generate an output signal as a division of clock

signal depending on the length and arrangements of bits [bit pattern] in shift registers [col. 2, lines 17 – 67, col. 3, lines 1 – 5, fig. 1].

It would have been obvious to one of ordinary skill in art, having the teachings of Svensson and Dellow before him at the time of invention was made, to modify clock generating system as disclosed by Svensson to include two shift registers as taught by Dellow, in order to obtain a clock generator configurable/programmable for odd, even or half integer division by detecting changes in the bit sequence and selectively deleting and allowing even, odd or half integer clock division [abstract, col. 1, lines 30 – 52].

22. As to claims 7 – 8, 15 – 16, and 23 – 24, Dellow discloses a two shift register frequency divider with a digital clock signal [reference clock] with multiplexer arrangement to select values from shift registers in alternating manner to generate an output signal as a division of clock signal depending on the length and arrangements of bits [bit pattern] in shift registers [col. 2, lines 17 – 67, col. 3, lines 1 – 5, fig. 1].

23. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested to the applicant in preparing responses, to fully consider the references in entirely as potentially teaching all or part of claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

24. **Prior Art not relied upon:** Please refer to the references listed in attached PTO-892, which is not relied upon for rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am to 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Nitin C. Patel
March 1, 2005